3. FELIX based test setup for FEB2

3.1. Software Installation

The server TANG (SSH login with felix@felix.phy.bnl.gov:3122) has been moved from the Rack to the test bench) for the test. Software and drivers are installed in directory /home/felix/software. The bitfiles for testing are put in ~/bitfiles/FEB2.

```
    ##########################################################################
    ###### Basic commands to access the FELIX firmware                  ######
    ###### kchen@bnl.gov                                               ######
    ##########################################################################
    flx-info # show basic status of the card
    # previous flx-monitor for checking of temperature, voltage, current and power of the optical modules has been integrated into flx-info
    flx-init # initialize the card with default configuration
    flx-config registers GWM # show GBT/LpGBT monitoring registers
    flx-config registers GWC # show GBT/LpGBT control registers
    flx-config set KEY=VALUE # write defined bit field in register
    flx-config get KEY # read defined bit field in register
    fpepo ADDR # read register raw data
    fpepo ADDR DATA # write register raw data
    # pepo is an obsoleted tool, for different firmware, the default Device ID and Vendor ID may need to be changed in source code, or be assigned when running; fpepo is suggested.
    pepo -u 1 -k -o ADDR -r -n 64 # read 64 bit register raw data
    pepo -u 1 -k -o ADDR -w DATA -n 64 # write 64 bit register raw data
    fdaq -T -t 2 -C testdata.dat # save data for 2 seconds, actually it is more than 2 seconds, data amount will be bigger than normal for the first second, since this tool needs initialization
    fflash -h # to update a relative finalized firmware to an assigned flash partition for FPGA, w/o JTAG
    flx-i2c -h # I2C configuration for on-board (BNL-712) I2C devices
    flx-reset -h # kinds of resets
```

3.2. Mapping and data format

3.2.1. Fiber mapping

The 48-ch FLX-712 card should be used for FEB2 test. Top MTP coupler close to the Timing Mezzanine should be used to connect the FEB2. The first two TRX links are for the 2 bidirectional control LpGBTx on FEB2. The other 22 RX links are for data. Meanwhile the trigger & clock fanout will be applied to downlink for these 22 transceivers. User can connect one of them to the FETB for pulse generation. For slice

testboard, 24-ch version will also works. Only the first 12-ch LpGBT links are in the top MTP coupler. User can connect the two MTP couplers, to verify whether the LpGBT links are locked in the firmware. Channels for the MiniPODs on the left side of FPGA (connected to the bottom MTP) are implemented with LpGBTx emulator.

3.2.2. Register map for FEB2 related functions

Table 1: FELIX Registers for the FEB2 Testing

Name	Address	Definition
ICEC_TRIG	0x6640	Trigger IC & EC operation
IC1_TXDATA1	0x6650	IC1 packet be sent: bit[63:0]
IC1_TXDATA2	0x6660	IC1 packet be sent: bit[127:0]
IC1_TXDATA3	0x6670	IC1 packet be sent: bit[191:0]
IC1_TXDATA4	0x6680	IC1 packet be sent: bit[255:0]
IC2_TXDATA1	0x6690	IC2 packet be sent: bit[63:0]
IC2_TXDATA2	0x66A0	IC2 packet be sent: bit[127:64]
IC2_TXDATA3	0x66B0	IC2 packet be sent: bit[191:128]
IC2_TXDATA4	0x66C0	IC2 packet be sent: bit[255:192]
EC1_TXDATA1	0x6720	EC1 packet be sent: bit[63:0]
EC1_TXDATA2	0x6730	EC1 packet be sent: bit[127:0]
EC1_TXDATA3	0x6740	EC1 packet be sent: bit[191:0]
EC1_TXDATA4	0x6750	EC1 packet be sent: bit[255:0]
EC2_TXDATA1	0x6760	EC2 packet be sent: bit[63:0]
EC2_TXDATA2	0x6770	EC2 packet be sent: bit[127:64]
EC2_TXDATA3	0x6780	EC2 packet be sent: bit[191:128]
EC2_TXDATA4	0x6790	EC2 packet be sent: bit[255:192]
FEB2_RELATED_CTRL	0x66D0	mode selection, and general control; and other functions
TRIGGER_DELAY	0x66E0	set trigger delay, rate and window size; and other functions
ADCSEL_CFG	0x66F0	choose ADC in single ADC mode; and other functions
ICEC_STATUS	0x7840	IC & EC operation status
IC1_RXDATA1	0x7850	IC1 packet received: bit[63:0]
IC1_RXDATA2	0x7860	IC1 packet received: bit[127:64]
IC1_RXDATA3	0x7870	IC1 packet received: bit[191:128]
IC1_RXDATA4	0x7880	IC1 packet received: bit[255:192]
IC2_RXDATA1	0x7890	IC2 packet received: bit[63:0]
IC2_RXDATA2	0x78A0	IC2 packet received: bit[127:64]
IC2_RXDATA3	0x78B0	IC2 packet received: bit[191:128]
IC2_RXDATA4	0x78C0	IC2 packet received: bit[255:192]
EC1_RXDATA1	0x78D0	EC1 packet received: bit[63:0]
EC1_RXDATA2	0x78E0	EC1 packet received: bit[127:64]

Continued on next page

Table 1: FELIX Registers for the FEB2 Testing

Name	Address	Definition
EC1_RXDATA3	0x78F0	EC1 packet received: bit[191:128]
EC1_RXDATA4	0x7900	EC1 packet received: bit[255:192]
EC2_RXDATA1	0x7910	EC2 packet received: bit[63:0]
EC2_RXDATA2	0x7920	EC2 packet received: bit[127:64]
EC2_RXDATA3	0x7930	EC2 packet received: bit[191:128]
EC2_RXDATA4	0x7940	EC2 packet received: bit[255:192]

- new bit field in these registers may be added;
- new registers may be added;
- 0x6640: ICEC_TRIG
  - bit[1:0], 1 per IC link, rising edge to trigger IC commands sending with following TXDATA registers.
  - bit[9:8], 1 per EC link, rising edge to trigger eC commands sending with following TXDATA registers.
- 0x6650-0x66C0: data for IC transmission. If users are sure for instance TXDATA4 (or more) are always 0xFFFFFFFFFFFFFFFF (or the packet ending delimiter 0x7E after useful data is in lower bits), then no need to update it in software, to reduce the times of register writing.
- 0x6720-0x6790: data for eC transmission. If users are sure for instance TXDATA4 (or more) are always 0xFFFFFFFFFFFFFFFF (or the packet ending delimiter 0x7E after useful data is in lower bits), then no need to update it in software, to reduce the times of register writing.
- 0x66D0: FEB2_RELATED_CTRL:
  - bit[0]: FIFO_RST, logic 1 to reset the two stages of FIFOs.
  - bit[1]: ENA, to enable the FIFO writing, and data transmission to PCIe.
  - bit[2]: LPGBT_FIFO_RST, logic 1 to reset the FIFOs between LpGBT and data organization module.
  - bit[8]: streaming mode: '0' is single ADC mode, '1' is trigger mode.
  - bit[9]: BCR_SEL, '0' use internal pseudo BCR, '1' use BCR from TTC system.
  - bit[16]: BCR_PHASE, set it as '1' will shift the 25ns pulse for 12.5ns, for all the 2-bit elinks to FEB2.
- 0x66E0: TRIGGER_DELAY:
  - bit[7:0], TRIGGER delay: delay the window for data taking, the unit is 1 BC.

  - bit[22:16], TRIGGER window size: how many samples per trigger. Bit field value 0-127 stands for 1-128.
  - bit[27:24], TRIGGER rate:
    * if bit 24 is 1, 40MHz/2^{16}.
    * else if bit 25 is 1, 40MHz/2^{15}.
    * else if bit 26 is 1, 40MHz/2^{14}.
    * else if bit 27 is 1, 40MHz/2^{13}.
    * else by default, 40MHz/2^{12}.
- 0x66F0: ADCSEL_CFG: bit[4:0], choose ADC in single ADC mode.
- 0x7840: ICEC_STATUS: only for reference. Bit[1:0], 1 per IC link. When IC transmission is started, it turns from 0 to 1; when the feedback packet from LpGBT is latched, it turns back to 0. Bit[9:8] are for the EC elinks in the two LpGBT links.
- 0x7850-78C0: similar as IC TXDATA, the quantity of reading operations may be reduce.
- 0x78D0-7940: similar as EC TXDATA, the quantity of reading operations may be reduce.

3.2.3. Data format per sample

Note: the sequence for the 32 bytes of each 256 bits below is reversed before sending. So ***fdaq*** saved data will show data from MSB to LSB.

- Trigger based mode.
  - 21x256 bits per sample (data is 32x160 bits, or 20x256 bits for ADC 0-31).
  - the first 256 bits:
    * bit[255:224]: 0xDEADBEEF
    * bit[223:160]: 0xAAAA555566669999
    * bit[159:96]: 0xFEDCBA9876543210
    * bit[95:89]: 0b0000000
    * bit[88]: ALIGNED (check the following 6 counters are same for 6 FIFOs after writing and reading)
    * bit[87:64]: 4 bits per counter. Same value is written to the 6 data FIFOs, check the readout values are still the same, if so the latency of these 6 FIFOs are the same.
    * bit[63:32]: event counter.
    * bit[31:23]: 0b000000000

117 * bit[22:16]: sample counter for current event.
118 * bit[15:12]: 0b0000
119 * bit[11:0]: internal BCID in FELIX firmware.
120 – the second 256 bits:
121 * bit[255:96]: data for ADC 31.
122 * bit[95:0]: data[159:64] for ADC 30.
123 – the third 256 bits:
124 * bit[255:191]: data[63:0] for ADC 30.
125 * bit[191:32]: data for ADC 29.
126 * bit[31:0]: data[159:138] for ADC 28.
127 – similar for following 18x256 bits.
128 • Single ADC mode
129 – 2x256 bits per 3 samples (ADC related data is 3x160 bits).
130 – the first 256 bits:
131 * bit[255:248]: 0x59
132 * bit[247:240]: counter, +1 per 3 BCs, used to align the two 256 bits frame.
133 * bit[239:80]: the data for the first sample in these 3 BCs.
134 * bit[79:0]: the bit[159:80] of the second sample in these 3 BCs.
135 – the second 256 bits:
136 * bit[255:248]: 0x6A
137 * bit[247:240]: same as in the first 256 bits.
138 * bit[239:160]: the bit[79:0] of the second sample in these 3 BCs.
139 * bit[159:0]: data for the third sample in these 3 BCs.
140 • 160 bits for each ADC
141 – bit[159:144]: FRAME8, or 0x0FA8 for fake data
142 – bit[143:128]: ADC-CH8
143 – bit[127:112]: ADC-CH7
144 – bit[111:96]: ADC-CH6
145 – bit[95:80]: ADC-CH5

- bit[79:64]: ADC-CH4
- bit[63:48]: ADC-CH3
- bit[47:32]: ADC-CH2
- bit[31:16]: ADC-CH1
- bit[15:0]: FRAME1, or 0x0FA1 for fake data

3.3. Quick checking of the functions

3.3.1. Quick test to verify the data transmission

```
    ###### Test of trigger base mode
    fpepo 0x66d0 0x102 # enable the data transmission to PCIe
    fpepo 0x66e0 0x7f0000 # transmit 128 samples per event
    fdaq -T -t 2 -C testdata.data # save 2 seconds of data; default internal trigger rate is
    ↪ 40M/4096, data rate is bigger than 800MB/s; if it saturate the disk writing, the
    ↪ trigger rate or samples per event should be decreased
    ###### Test of continuous mode for single ADC (160 bits per ADC per sample)
    fpepo 0x66d0 0x2 # enable the data transmission to PCIe
    fdaq -T -t 2 -C testdata.data # save 2 seconds of data; data rate is also bigger than 800
    ↪ MB/s; PC memory will guarantee no data loss for a few seconds even if the disk
    ↪ writing is slow
```

For real test, it is better to disable the data transmission to PCIe in the firmware, then open ***fdaq***, then enable data stream after some time sleep. Trigger based mode should be used for most of the testing. Single ADC mode may be useful for FFT and ADC dynamic performance analysis. Below code is the example to take trigger mode data and single ADC data.

```
import os,time
os.system("fpepo 0x66d0 0x100") # disable stream
os.system("fpepo 0x66e0 0x7f0000") # 128 samples per event
cmd = "fdaq -T -t 2 -C allADC.dat &"
os.system(cmd)
time.sleep(0.5)
os.system("fpepo 0x66d0 0x102") # enable stream
```

```
import os, time
os.system("fpepo 0x66f0 0x0a") # change to ADC10 with fake data
os.system("fpepo 0x66d0 0x0") # disable stream
cmd = "fdaq -T -t 2 -C singleADC.dat &"
os.system(cmd)
time.sleep(0.5)
os.system("fpepo 0x66d0 0x2") # enable stream
```

In current firmware, for the unused 24 ADCs, fake data with counter are streamed.

3.3.2. LpGBT links verification

The 24 links are tried to connect with the VLDB+, for all links with light, bidirectional links are locked. Since local 40M is for LpGBT RX decoding, the firmware doesn't rely on the first RX link. Some links from the FLX-712 via fiber and patch boxes have no light, issues may come from the 48 to 4x12 fiber or patch box. The card used is the 48-ch card in server HAN. For future test slice testboard test, the 24-ch card in server TANG will be used.

The Tx & Rx links with VTRX+ are as below, with one half of the 2xMTP-12 to 24 LC patch box :

Label on the patch box	6	5	4	3	2	1
			from VLDB+			
				to VLDB+		

3.3.3. IC function

The IC links of LpGBT link 2 was verified. Code in https://gitlab.cern.ch/BNL-ATLAS/larphase2/analog_testboard/analog_testboard_debugging_software/-/tree/master/hdlc_ic_python_flx_tool can be used as an example. But the register address and bit field in ICOP_analog_tb_version.py should be changed to match above register table.

```
python ICOP_analog_tb_version.py -s 0x70 -a 0x0034 -l 1 -r # read register 0x0034
```

Bit order of the 2 IC bits for LpGBTx are same with EC bits of GBTx, and different with IC bits of GBTx. The new developed software will focus on the VLDB+, to control GPIO and I2C.

3.3.4. Trigger distribution to FETB

Trigger is sent to the IC bits of link 2-23. It is verified on ZC706, which can recover the trigger and generate pulse control signal with fix latency, compared to the recovered 25ns wide trigger.

3.3.5. Default mode

The LpGBT default mode in firmware is configured to be 10.24 Gbps and FEC5 for uplinks. However flx-init will change it to 5.12 Gbps and FEC5 mode (Registers 0x6580-0x65B0 are all 0xF). 0x6580 and 0x65A0 are for line rate control. 0x6590 and 0x65B0 are for FEC mode selection. User can change 0x6580 and 0x65A0 to 0xFFFFFFFFFFFF after flx-init for 10.24 Gbps.

3.3.6. Other ADC data elinks

See other documents for more details. For slice testboard, the elink mapping firmware is designed for below fiber mapping: The LpGBT12 should be connected to CH0 of FELIX; LpGBT13 => CH1; LpGBT9 => CH12; LpGBT10 => CH3; LpGBT11 => CH4; LpGBT14 => CH5; LpGBT15 => CH6; LpGBT16 => CH7.