NEVIS LABORATORIES
COLUMBIA UNIVERSITY

TEXAS
The University of Texas at Austin

COLUTAv4 Update

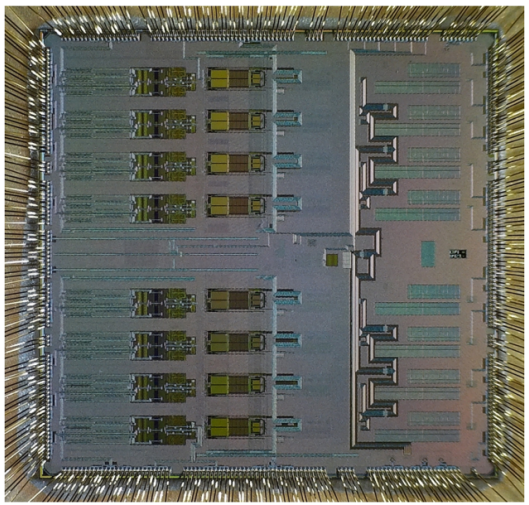
Gabriel Matos
O.B.O the COLUTA Team
May 11, 2022

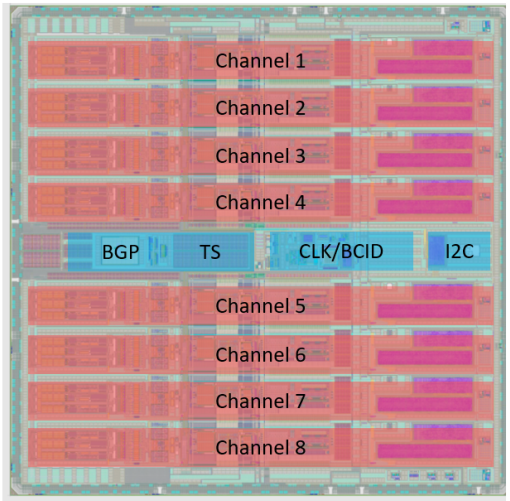
ATLAS
EXPERIMENT

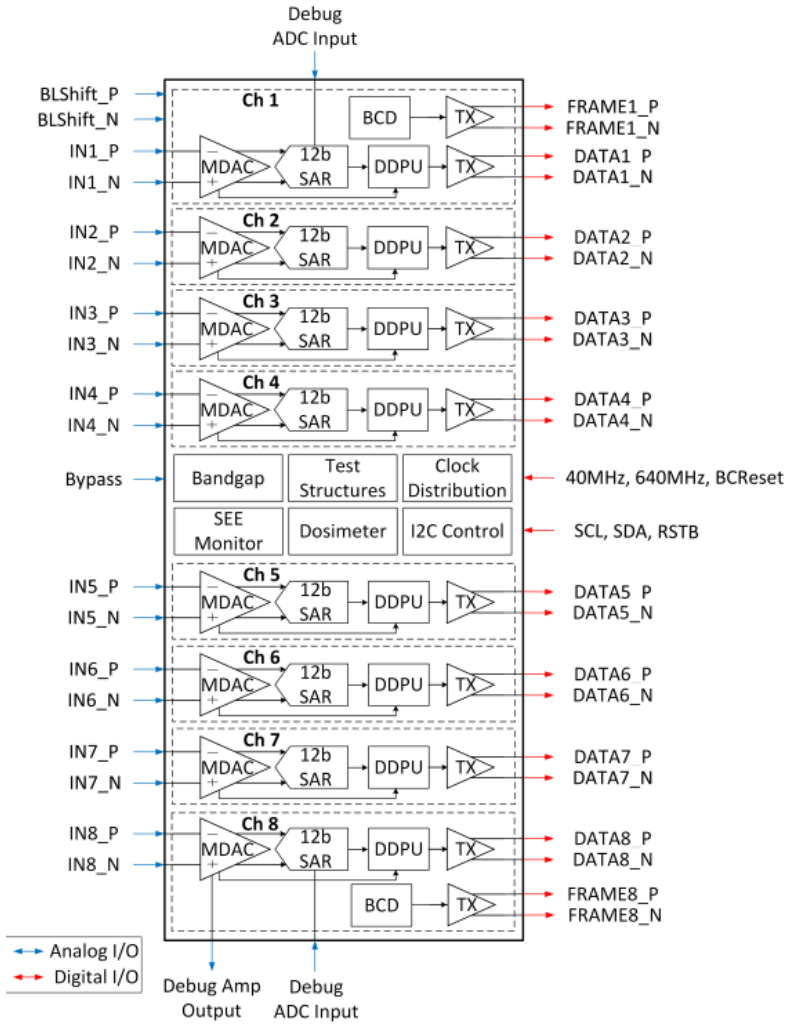
1. COLUTAv4 ADC & Testboard Overview
2. Performance Testing
3. Status of BGA, Radiation & Production Testing
4. Conclusions

COLUTAv4 ADC

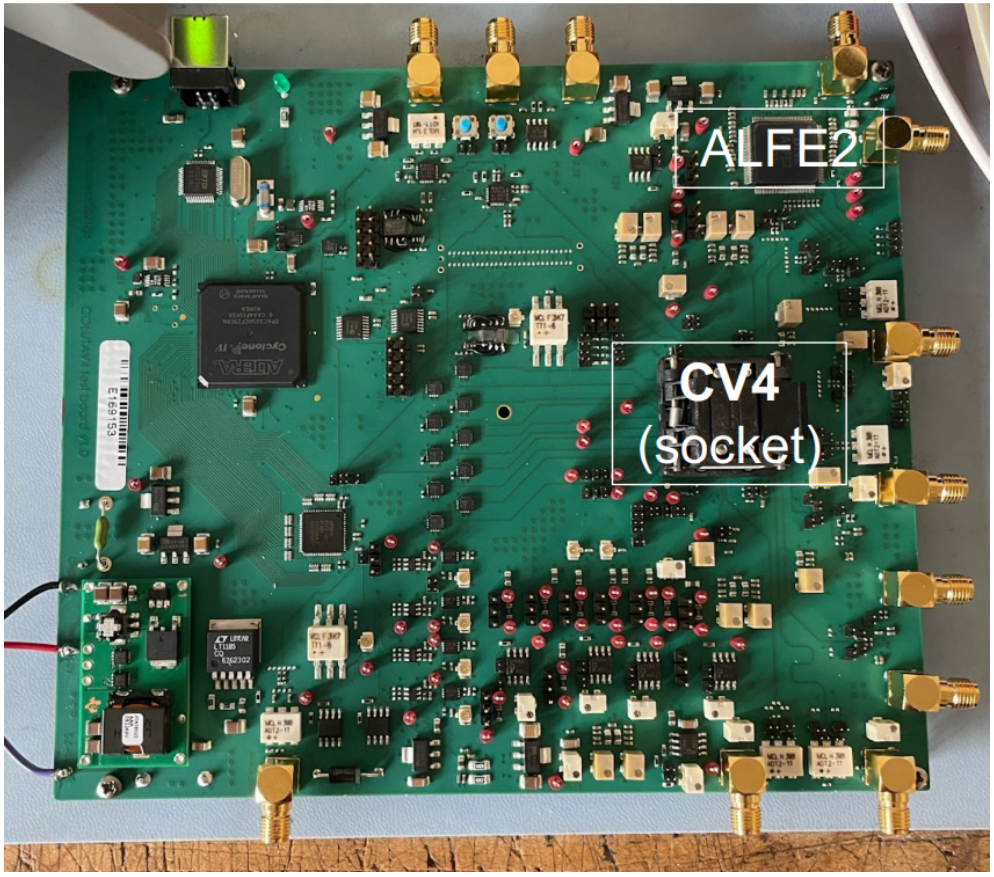
- 8-channel, 15-bit, A/D converter
  - Channels are identical MDAC+SAR+DDPU
- Digitizes both gains of LAr calorimeter channels
  - Digitization at 40 MSPS, w/ >11-bit precision
  - Seamless interface to PA/S, lpGBT serializers
- TSMC 65nm LP CMOS
  - 5.584 x 5.456 mm^2 chip die
  - 4.3 million transistors
  - 1.2 V operation with 2 V_{pk-pk} differential input







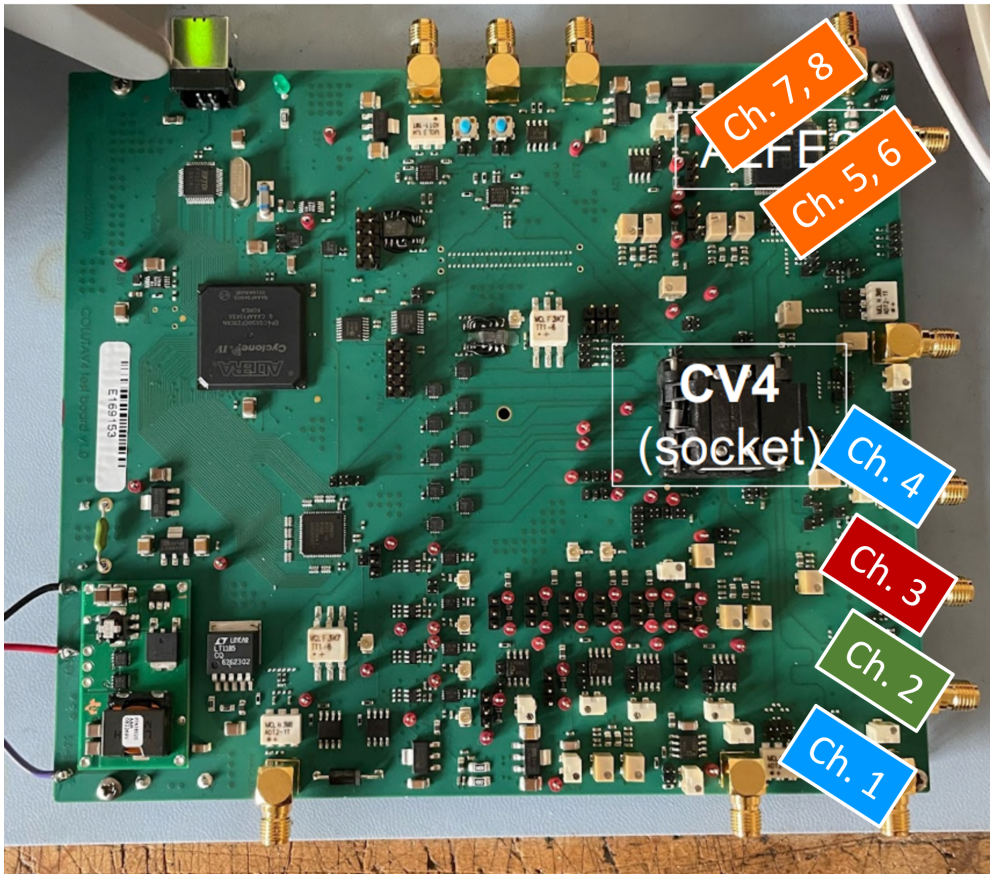
COLUTAv4 Testboard & Timeline



- Chips submitted Sept. 1st
- 100 chips ordered in total
  - 20 packaged in QFN100 received Dec. 20th
  - Other 80 will be packaged in BGA
- 2 first testboards assembled early Feb.
  - Socketed board for initial testing with option to solder down
  - Includes ALFE2 for PA/S integration
- Testing begun in late-Feb.
  - Preliminary results shown in March LAr Week
  - Since then 2 additional boards arrived

- This talk will provide an overview of recent CV4 test results and next steps
  - Including very preliminary integration results with PA/S!

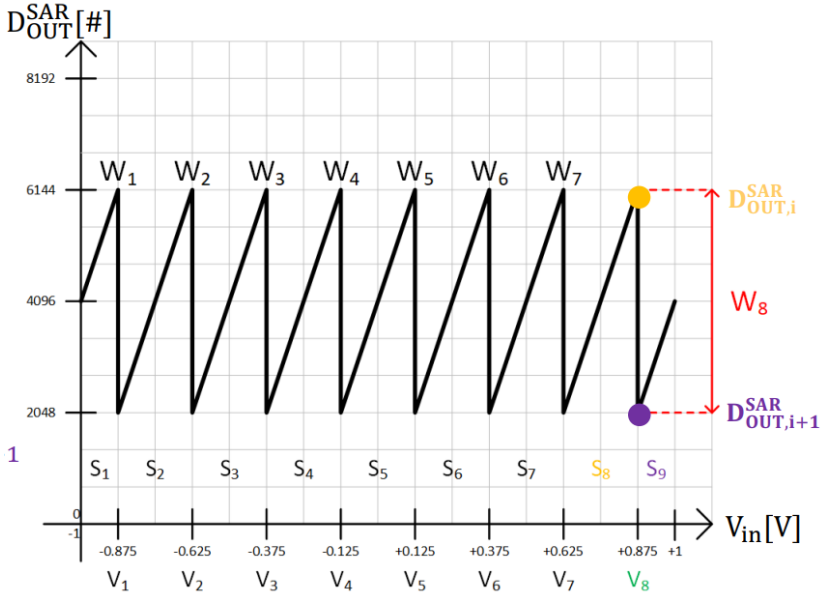
Test Setup

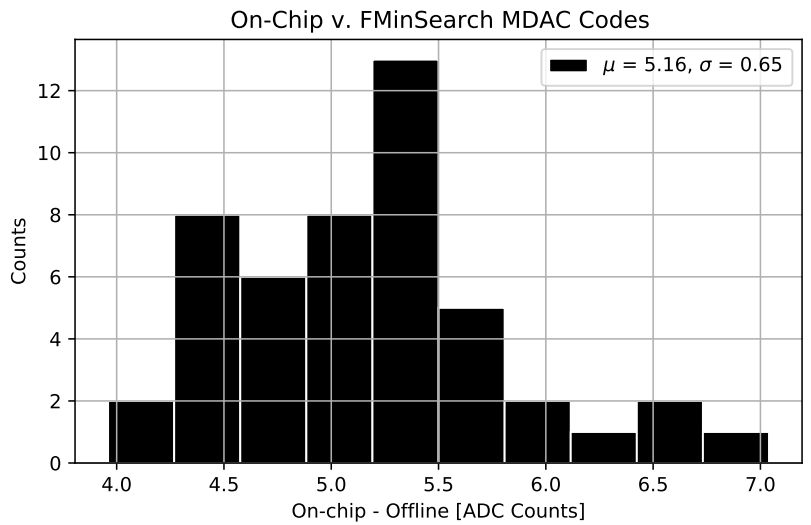


- CV4 testboard channel layout
  - Chs. 1, 4: transformer input
  - Ch. 2: commercial amplifier input
  - Ch. 3: connected to onboard DAC
  - Chs. 5-8: connected to ALFE2
    - Chs. 6, 7: hi gain
    - Chs. 5, 8: lo gain
- Input signals provided by AWG
  - Connected directly to board with filter (for sine tests) and/or attenuators
  - Generates sine and LAr pulses
- DAC used for linear ramp input
- MDAC+SAR calibration performed with on-chip circuit
- Performance assessed for all 20 chips

Optimization of MDAC On-Chip Weights

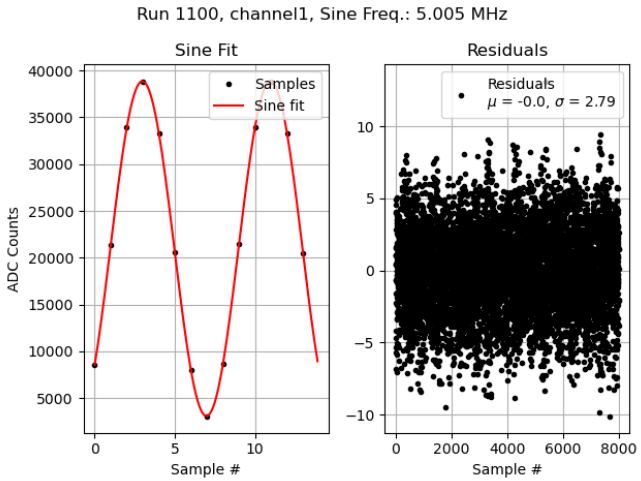
- On-chip MDAC calibration
  - MDAC contains 9 distinct subranges
  - Calibration processes “stitches” together subranges with a set of 8 weights to create a linear transfer function
  - Weights derived from on-chip circuit
- Offline (FMinSearch) calibration
  - Offline “fitted” calibration derives weights to yield best possible sine performance
  - Used only to debug on-chip process
- On-chip calibration constants systematically ∼4-5 counts lower than offline constants
  - True for multiple CV4 channels and chips
  - Reason for this still under investigation...
  - For now added 4 count empirical offset to on-chip calib. for improved performance

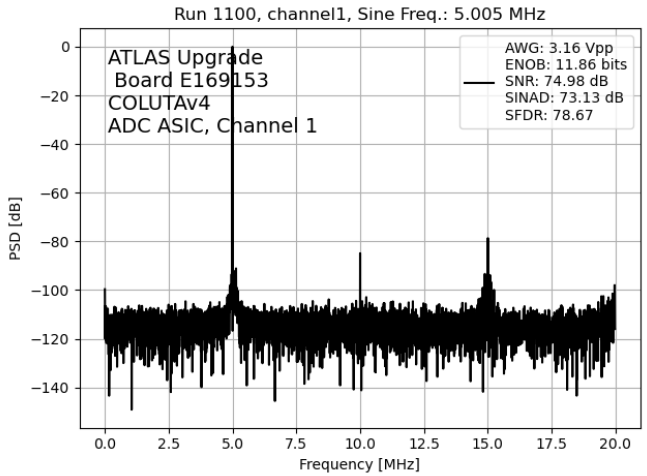




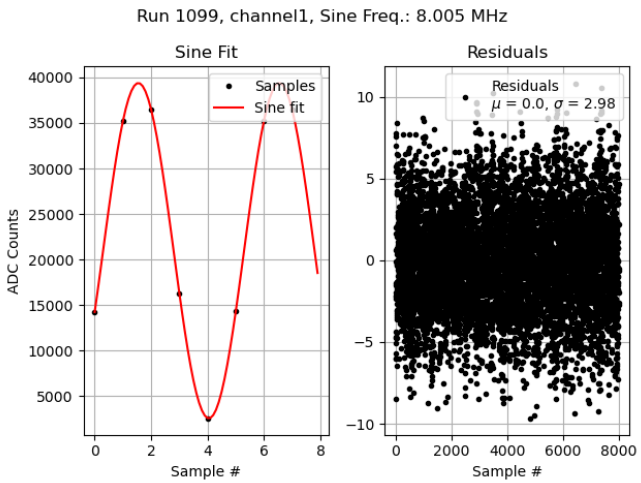
Sine Wave Performance: Fits & FFTs

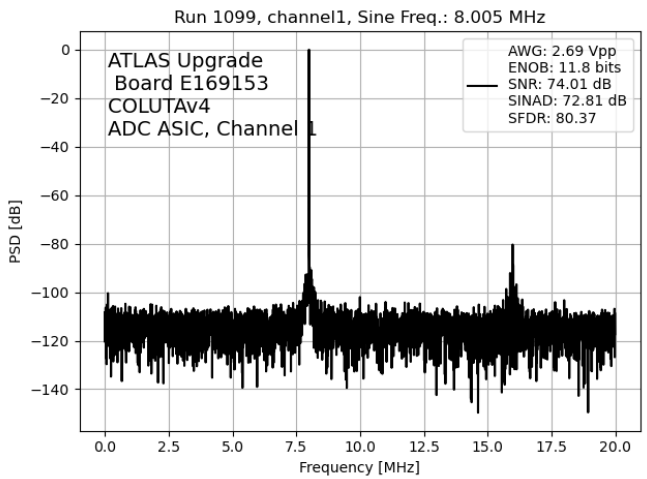
- Sine performance characterized fully with offset on-chip calibration
  - Sine fits (shown in red) and residuals for 5, 8 MHz inputs
  - FFTs at roughly full scale show >11.5b ENOB (spec. >11b @ 8MHz)





Freq.: 5.005 MHz
11.86 ENOB

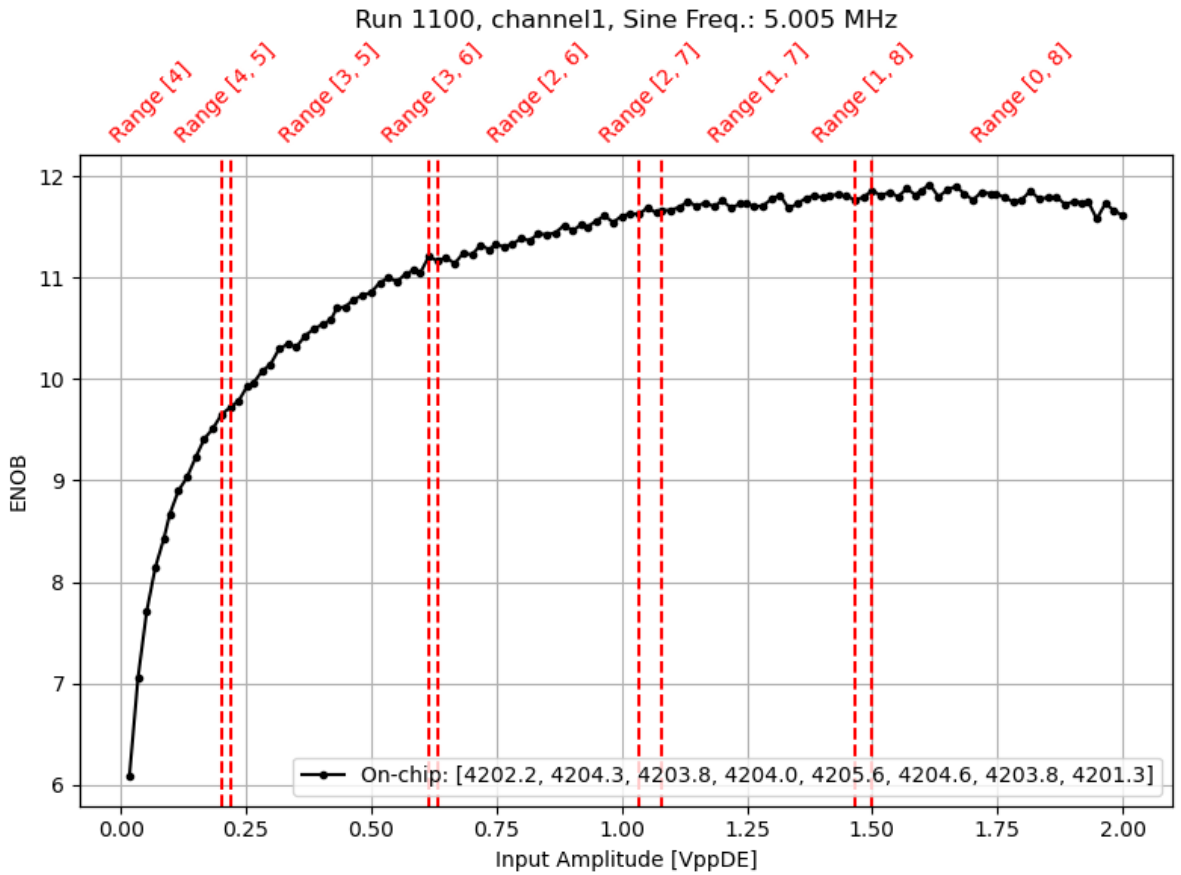




Freq.: 8.005 MHz
11.8 ENOB

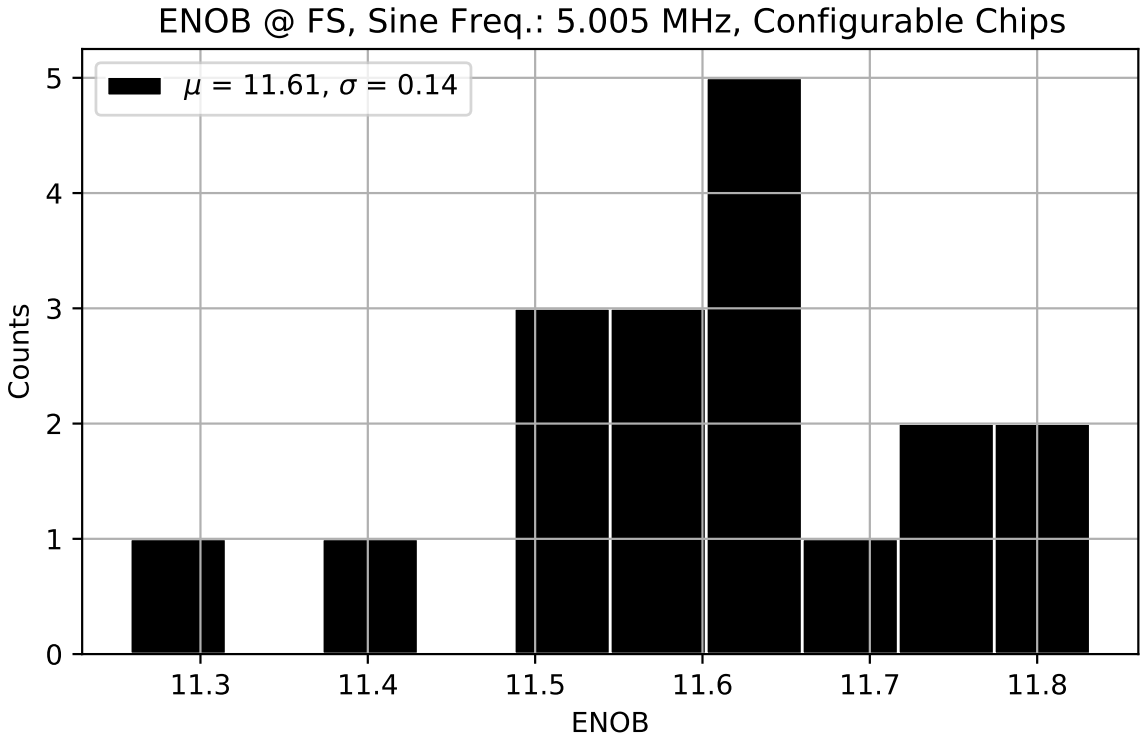
Sine Wave Performance: ENOB v. Amplitude

- Scan performance across input range by varying amplitude of the sine signal
  - On-chip calibration shows >11b performance for >500mVpp differential input
  - No noticeable kinks at MDAC transitions (in red) as had been seen with CV3
- Performance exceeds spec. across entire relevant frequency range as well



Sine Performance Across Chips & Yield

- Tested all 20 packaged chips → 18/20 chips configurable!
  - Investigating remaining two, may be possible to recover
- Configurable chips show good performance out-of-the-box
  - Sine performance on channel 1 at ∼full scale >11b ENOB with on-chip calibration
  - On-chip calibration results shown here *without* offset → still above spec.



DNL & INL Measurements

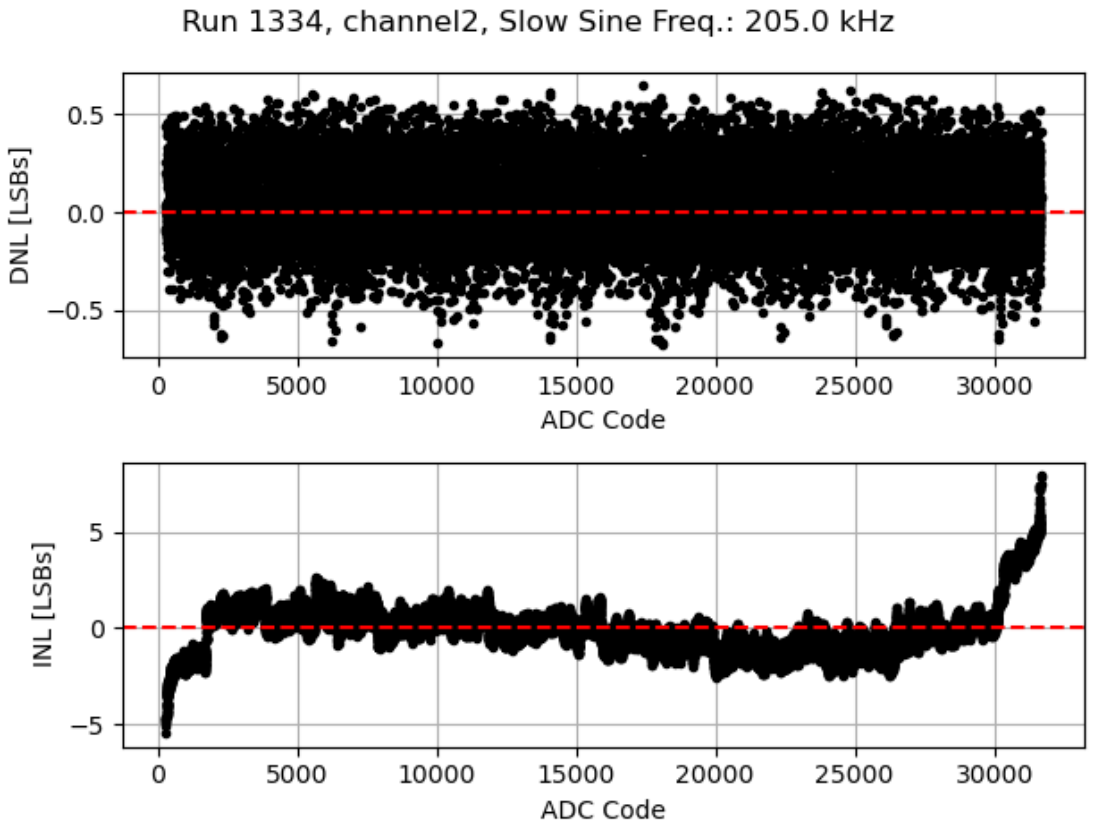
- Slow sine input (~200 kHz) used to test for nonlinearity
- DNL computed from linearized transition voltages V_j and INL from linear fit
  - Results (shown in 15b LSBs) show no missing codes

$$\mathrm{DNL}_j = \frac{V_{j+1} - V_j}{1\ \mathrm{LSB}} - 1$$

-0.67/+0.65 15b LSB
(-0.07/+0.08 12b LSBs)

$$\mathrm{INL}_j = \frac{V_j - V_{\mathrm{fit},j}}{1\ \mathrm{LSB}}$$

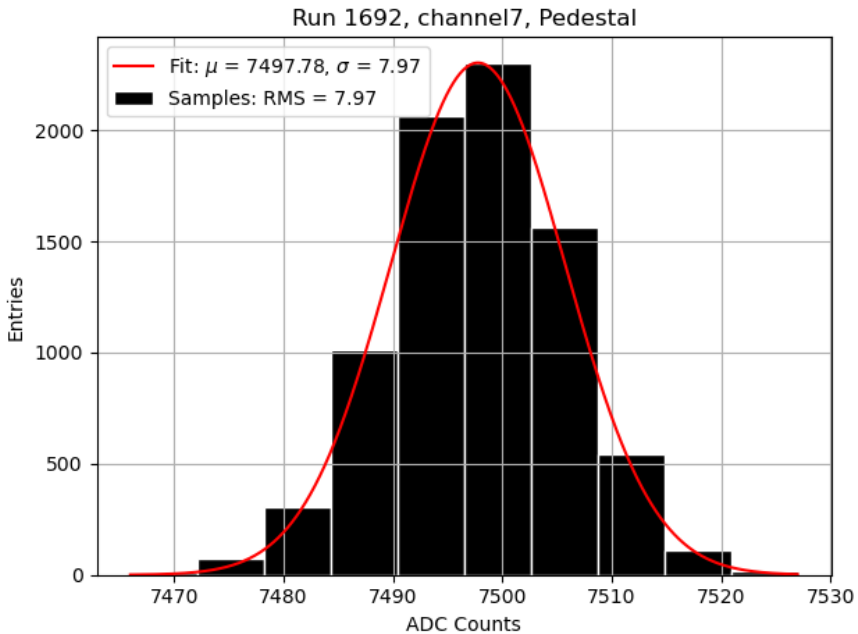
-5.51/+7.98 15b LSB
(-0.69/+1.00 12b LSBs)

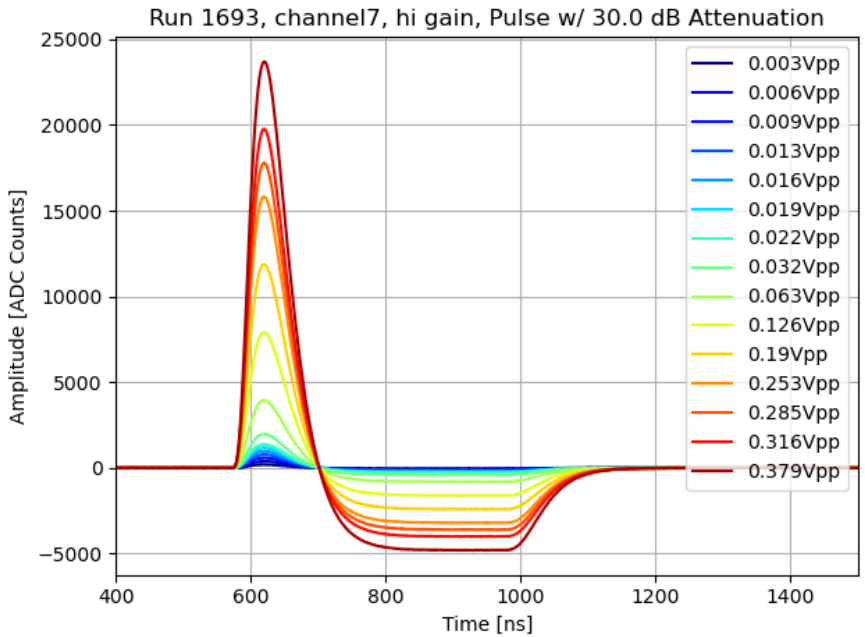


- DNL -0.07/+0.08 (spec. -1.0/+1.0 12b LSBs), INL <0.03% (spec. <0.1%)

Preliminary PA/S Integration: LAr Pulses

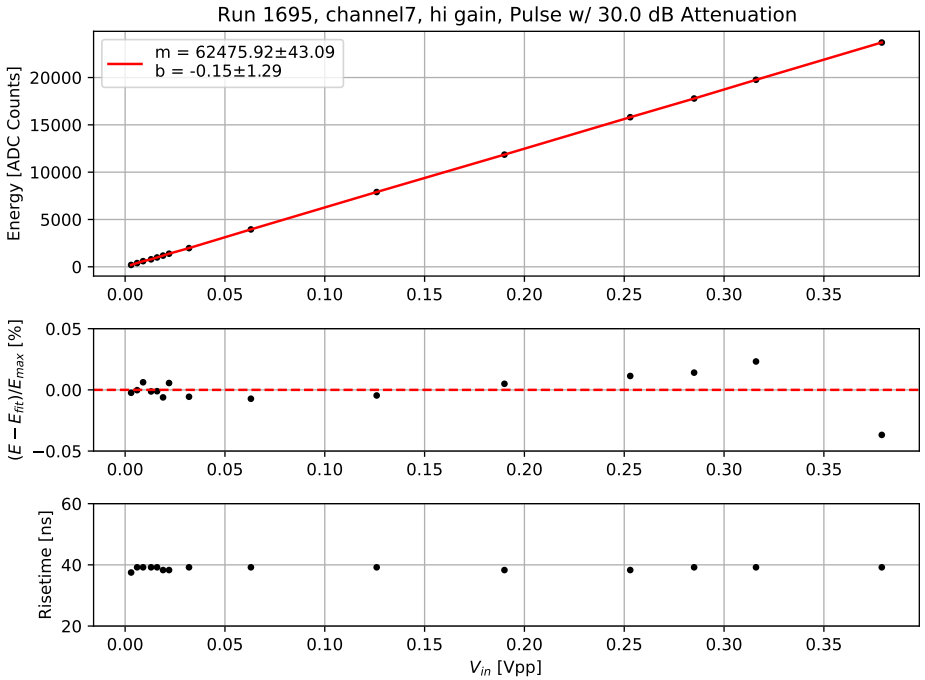
- Have been able to successfully talk to and configure the ALFE2
  - ALFE2 set to recommended settings
  - 25Ohm, 1nF capacitance load configuration
  - Pedestal noise of ∼8 counts (hi gain) and ∼2.5 counts (lo gain)
- Pulses sent from AWG onto ALFE2 channels (CV4 chs. 5-8)
  - 30 pulses interleaved to create fine resolution pulse for OFC analysis
  - Calibration provides smooth pulse shape and derivative, including across MDAC transitions (see backup)

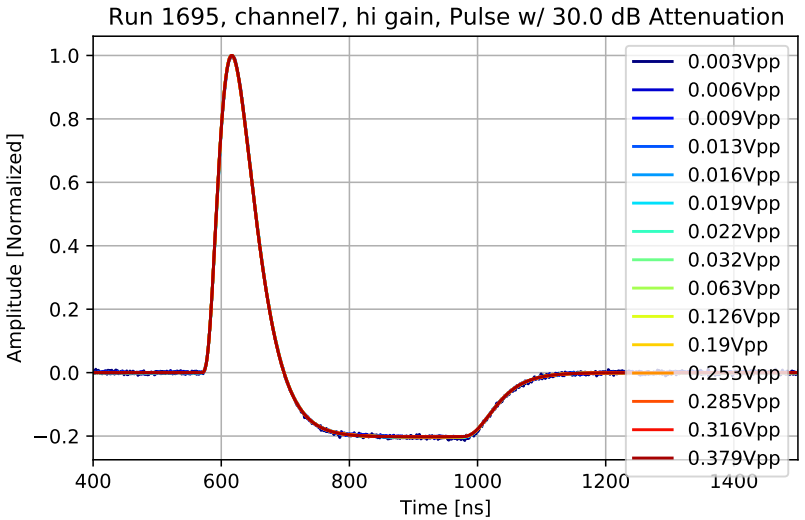




Pulse Shape and Linearity

- All measurements still very preliminary, but promising
  - More careful quantitative studies to follow over next few months

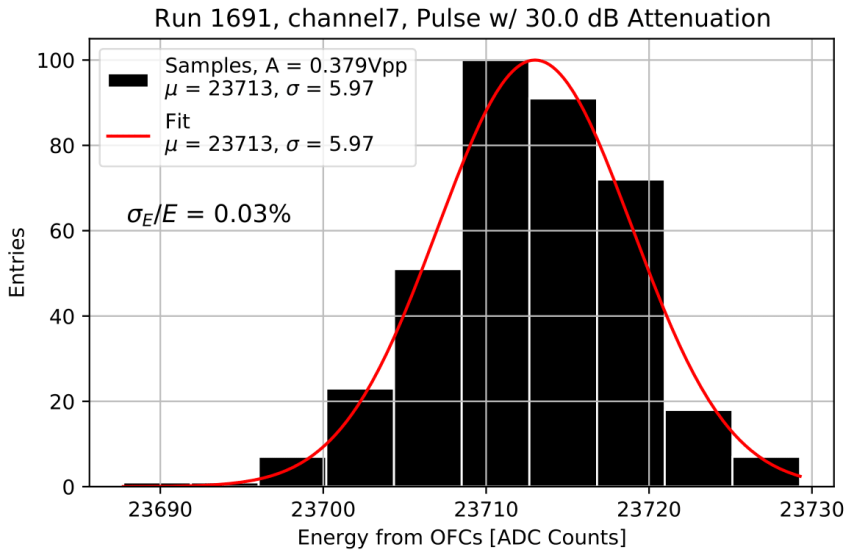


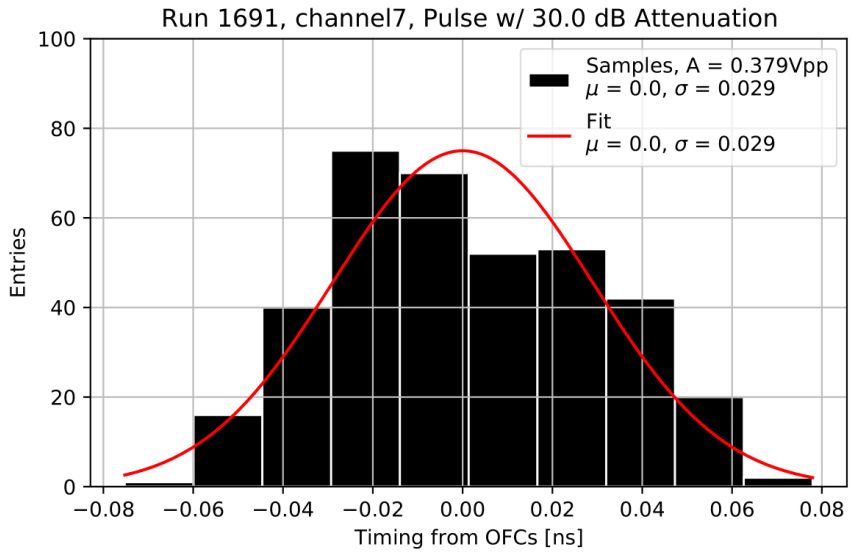


- Normalized pulse shapes show no distortion across a range of input amplitudes
- Pulse nonlinearity <0.05% across dynamic range (spec 0.1% up to 60% full dyn. range, 1% at 80% full dyn. range, <4% at 100% full dyn. range)
  - Risetimes ∼40ns and gain ratio of ∼21.2 for current configuration

Energy and Timing Resolution

- Use fine pulse to compute OFCs (as outlined here) and apply to large pulse close to saturating ADC to determine energy and timing





- Preliminary achieved resolutions
  - σ_E/E = 0.03% (spec. $\sigma_E/E < 0.25\%$)
  - σ_t = 29 ps (spec. σ_t < 100 ps)
    - This is dominated by jitter of trigger signal from on-board FPGA, not ADC

Investigating Multichannel Calibration

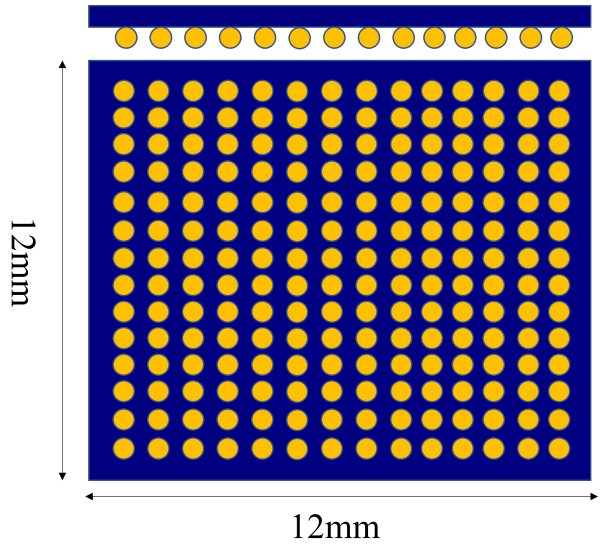
- Currently MDAC+SAR calibration is performed one channel at a time
  - In the end will have ~1524 FEB2 boards each with 32 COLUTA chips
  - Calibration process can take a long time even at the single-board level
- Preliminary investigation on calibrating multiple channels simultaneously
  - SAR architecture requires even/odd channels be calibrated separately
  - In CV3, even/odd calibration led to syst. shift (+4 to 5 counts) in MDAC constants
  - Changes to calibration circuit in CV4 implemented to prevent this

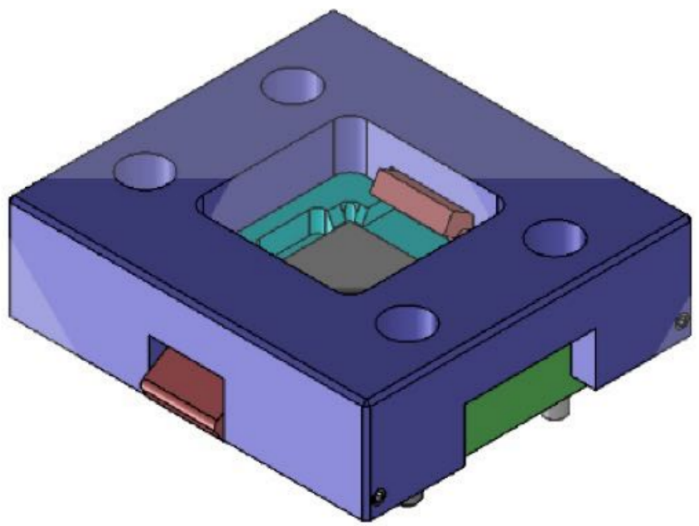
Calibration Mode	MDAC Weights							
Single Channel	3929.1	3931.4	3930.9	3930.8	3931.7	3931.1	3929.5	3928.1
Even/Odd	3930.5	3931.8	3931.8	3931.4	3932.8	3931.9	3930.6	3929.6
Diff.	+1.4	+0.4	+0.9	+0.6	+1.1	+0.8	+1.1	+1.5

- On avg. <1 count difference between single channel and even/odd calibration
  - Preliminary conclusions, studies still ongoing...
- Both sets of constants yield comparable sine performance (see backup)

COLUTAv4 BGA Packaging

- BGA production in final steps of approval
  - Vendor selected and all paperwork submitted
  - Vendor schedule compatible with our pre-production requirements
- BGA packaging specifications
  - Low profile fine pitch BGA
  - Ball pitch: 0.8 mm
  - Size: 12x12 mm
  - Pin count: 196
- Vendor is the same for PA/S chip
  - Will coordinate on test sockets
  - Initial studies on socket type in progress
    - Open top
    - SMD only (chip can be soldered)
    - Qualified for 500k to 700k cycles
    - Can be automatically cleaned
    - Pogo pins qualified for 300k to 500k cycles
    - Manufacturer: VA Innovation

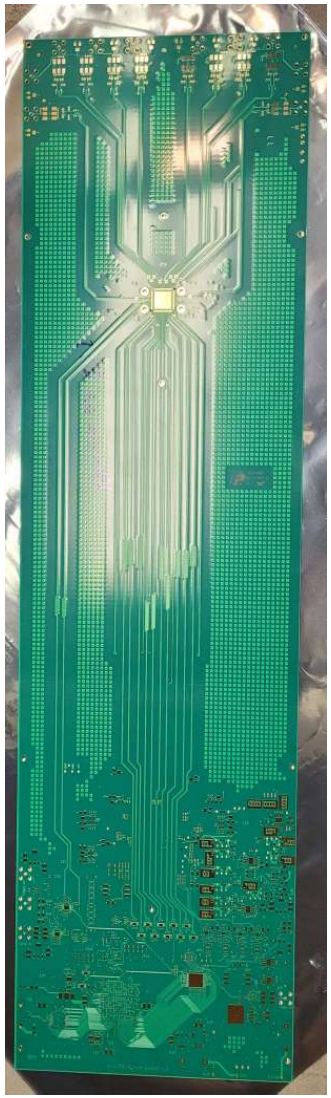




Radiation Testing

- Radiation board PCBs fabricated!
  - Being assembled with a ∼3 week delivery quote (though we have seen delays in assembly)
- Radiation testing scheduled at MGH (Boston)
  - Dates currently set for Aug. 5/6th
  - Will repeat radiation performance tests done for CV3
    - Connect onboard DAC to CV4 input
    - Set DAC to analog code
    - Digitize samples with CV4 and histogram
    - Repeat for next DAC code
  - Focus on SEE tests → improved mitigation in digital blocks w/ new, larger spacing for redundant logic

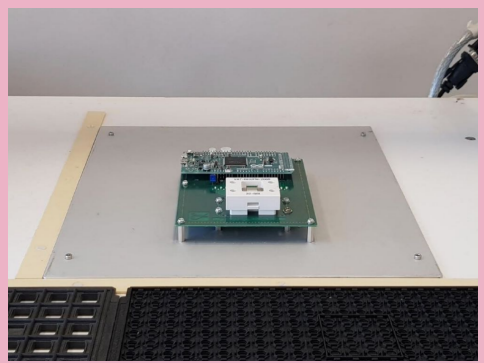
CV3 Test Setup



Production Testing

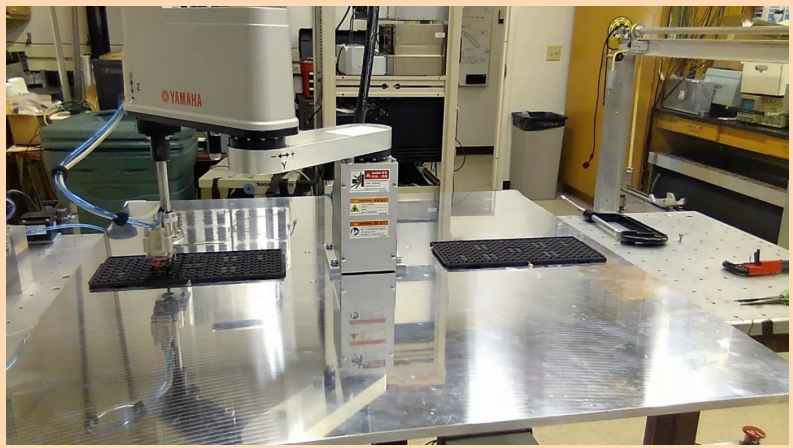
- Preparing for production testing of ∼80k chips
- Multiple institutions contributing to the testing program
  - CV4 board sent out to Austin collaborators last week
  - Another will go to collaborators in Saclay in the near future

Paris-Saclay



- Existing robotic test setup being prepared for testing
- Initial socket testing studies

Austin



- Assembling robotic arm setup
- Long duration tests checking placement of “dummy” chips

Conclusions

COLUTA: Custom 8-Channel 15-bit 40-MSPS ADC for the ATLAS Liquid Argon Calorimeter Readout

Rui Xu, Jaroslav Ban, Sarthak Kalani, Chen-kai Hsu, Subhajit Ray, Brian Kirby, Gabriel Matos, Julia Gonski, Andrew Smith, Devanshu Panchal, Michael Unanian, Xiangxing Yang, Nan Sun, John Parsons, Timothy Andeen, Peter Kinget

- Continued testing of CV4 chips since LAr Week
  - Characterized sine performance, nonlinearity, and calibration → all meet specs!
  - Tested multiple chips with 90% yield thus far
  - Early integration with ALFE2 shows promising results
  - Some features (i.e. offset to calibration constants) still need to be understood
- BGA production in final steps of approval and soon to be underway
- PCBs for radiation test received and being assembled now
- CV4 board sent out to Austin and progress towards production testing
- Paper submitted to IEEE NSS after discussion with LAr Speakers Committee

Thank You!

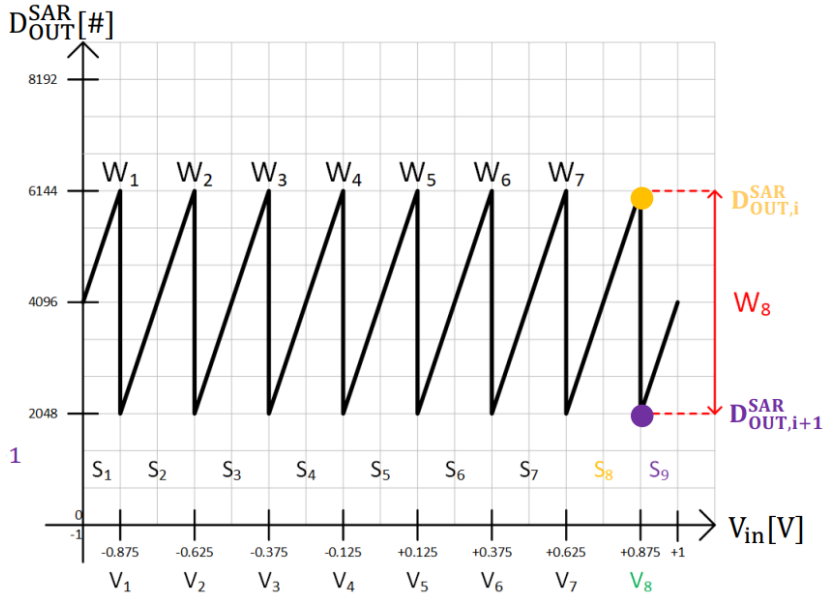
Backup

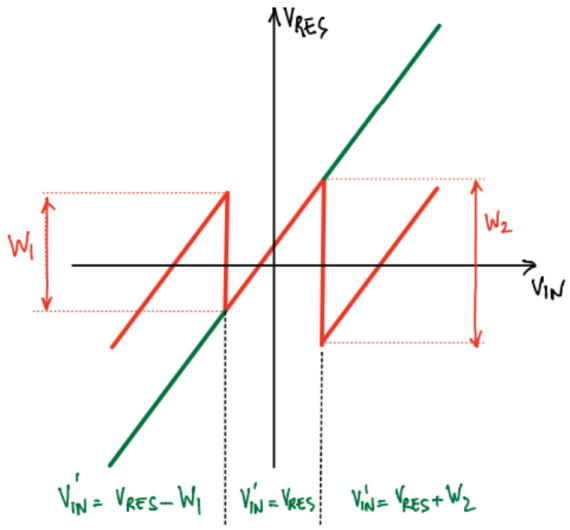
MDAC Calibration Process

- Procedure
  1. Assert V_i
  2. Force S_i
  3. Measure $D^{\text{SAR}}_{\text{OUT},i}$
  4. Force S_{i+1}
  5. Measure $D^{\text{SAR}}_{\text{OUT},i+1}$
  6. Calculate $W_i = D^{\text{SAR}}_{\text{OUT},i} - D^{\text{SAR}}_{\text{OUT},i+1}$
  7. Repeat for i = 1 to 8
- DDPU uses $W_1, \ldots, W_8$ to "stitch together" subranges ande create a linear transfer fcn.

$$D^{\text{MDAC+SAR}}_{\text{out}} = D^{\text{SAR}}_{\text{out}} - 4096 + \sum_{i=1}^{8} W_i \cdot b_i$$

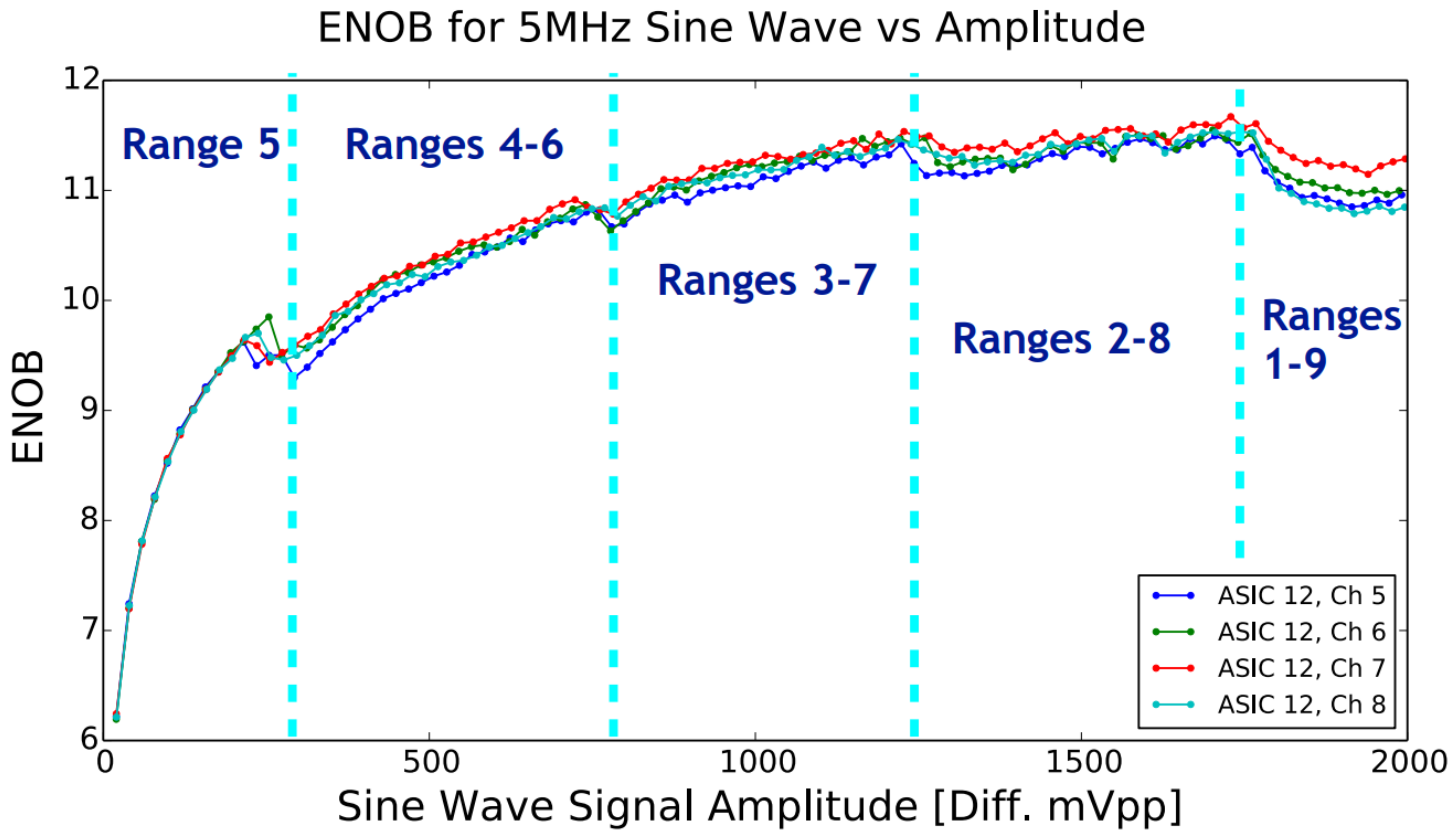
- All calibration circuitry is on-chip
- MDAC calibration is done after SAR calib.





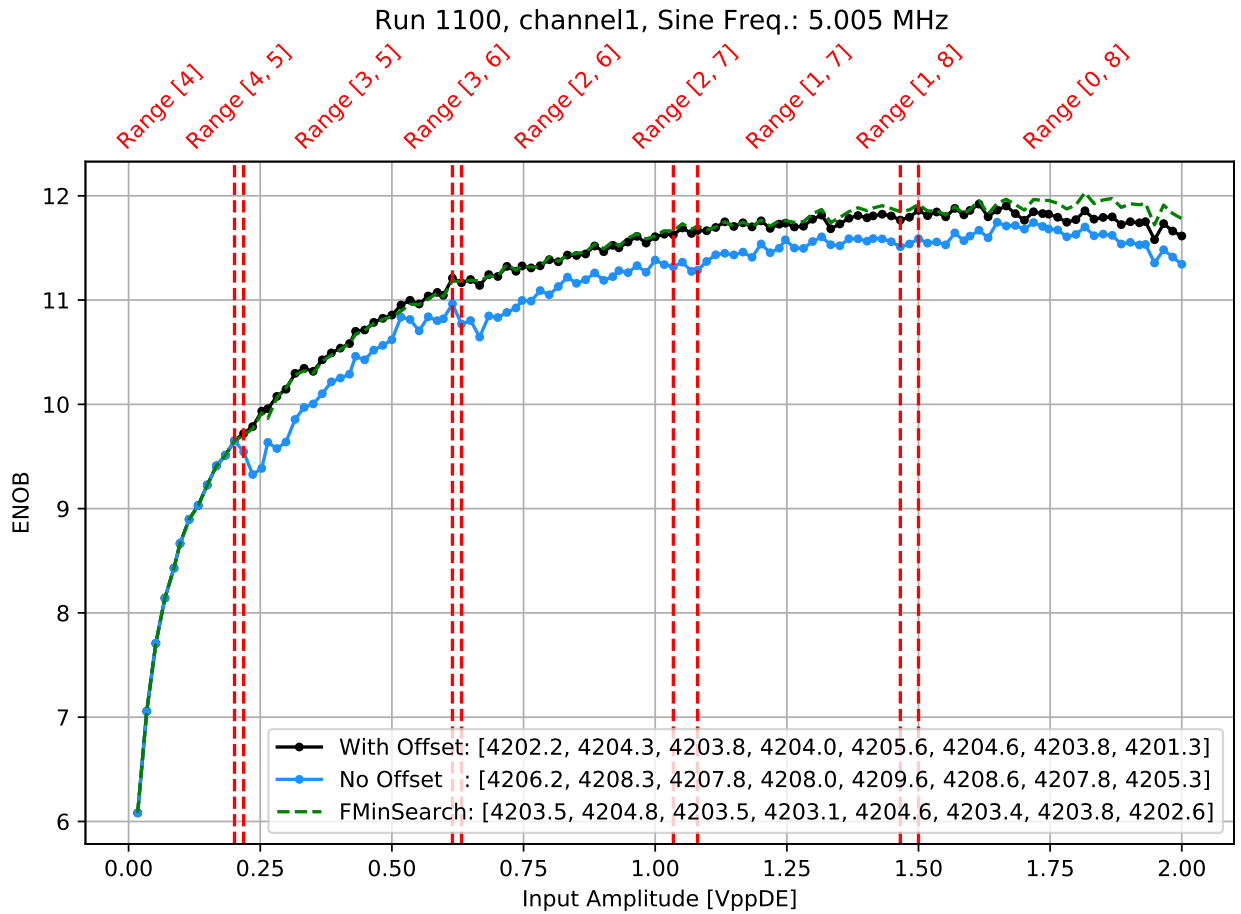
CV3 ENOB v. Amplitude

- Dips in ENOB at MDAC transitions (shown in cyan) show instances where the on-chip calibration does not properly stitch the subranges together
- Additional clock phase added into the MDAC resets the sampling capacitor after each cycle and eliminates the transition offset dips in CV4



Performance With/Without Calibration Offset

- Without MDAC calibration offset of -4 counts begin to get dips at MDAC subrange transitions (shown in red) as in CV3 case
  - Even with “non-optimized” calibration constants, dips are smaller than CV3 case and still achieve >11b ENOB after 750 mVppDE and >11.5b ENOB at full-scale

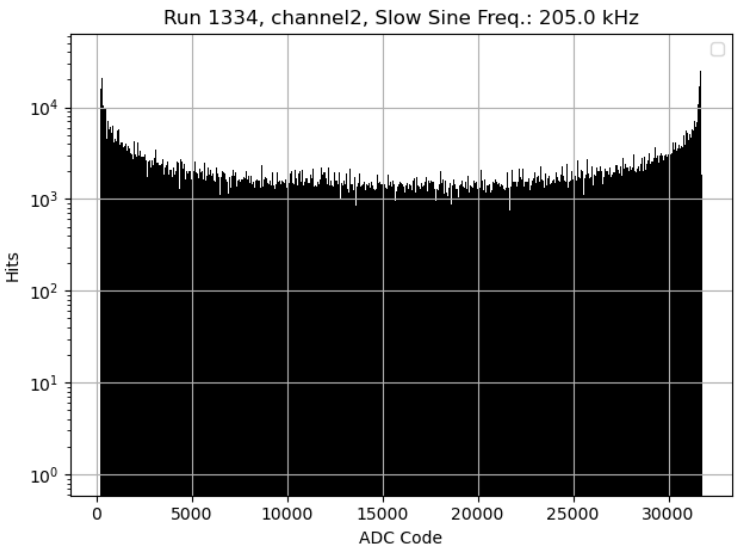


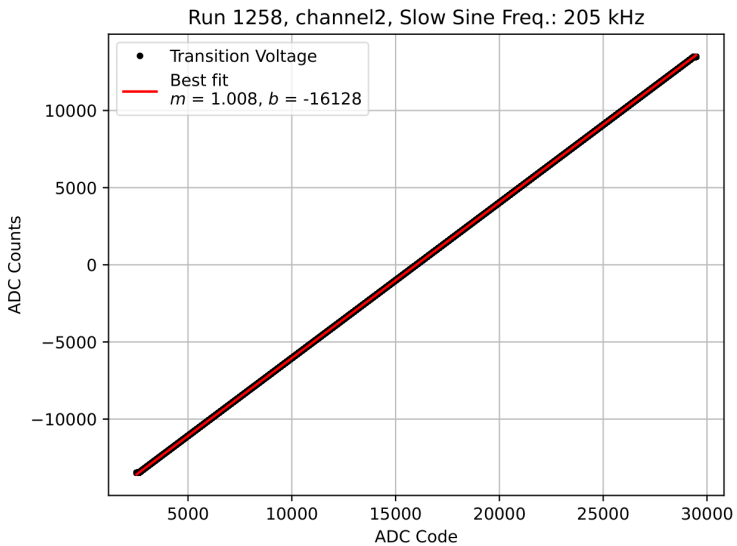
Slow Sine DNL/INL Methodology

- Derive transition voltages (method outlined in this document)

$$V_j = -A\cos\left(\frac{\pi}{M}\sum_{k=0}^{j} H_k\right)$$

$A =$ amplitude in ADC counts
$M =$ total number of samples
$H_k =$ contents of kth sine histogram bin

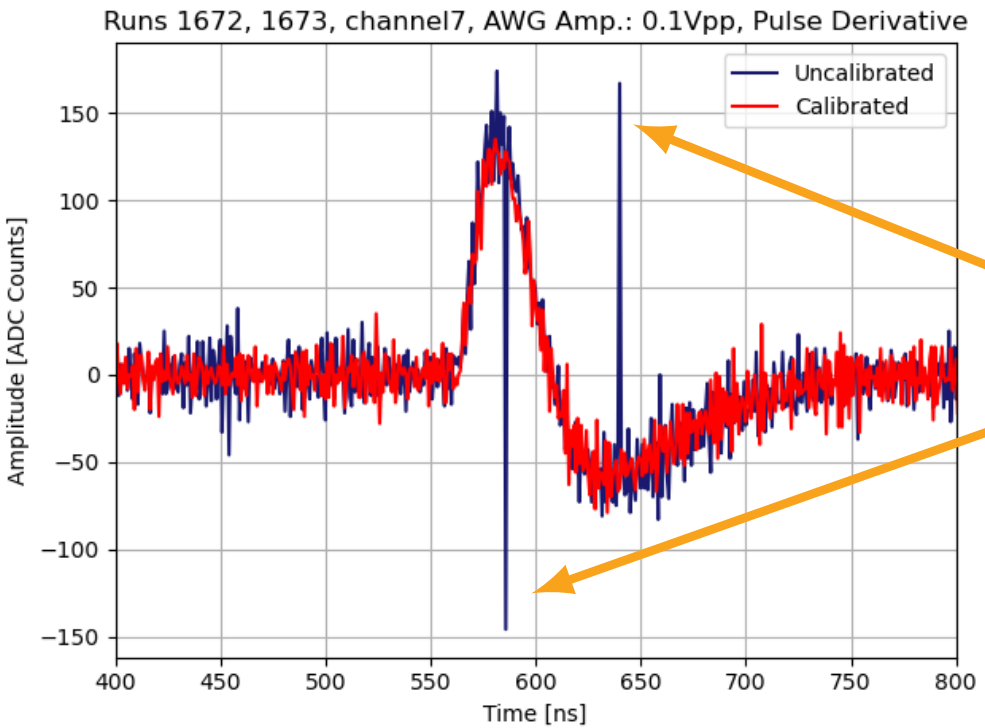




- Transition voltages takes sine histogram (left) and linearizes it (right)
- Use to define $\mathrm{DNL}_j = \frac{V_{j+1}-V_j}{1\ \mathrm{LSB}} - 1$ and $\mathrm{INL}_j = \frac{V_j - V_{\mathrm{fit},j}}{1\ \mathrm{LSB}}$

LAr Pulse Derivative

- Visualizing MDAC calibration removing transition offsets in LAr pulse
  - An MDAC offset shows as a large spike in the derivative of the interleaved pulse
  - Calibration process removes offsets, producing a smooth pulse derivative



MDAC Transition

Single Ch. v. Even/Odd Calibration Performance

- Sine performance with both on-chip single channel (series) and even/odd calibration comparable to ideal performance using fitted weights

Artifact due to AWG